Standard Agent Interface

Reference Guide

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Specifications

Purpose

This document describes the external interfaces of the Content Processing Controller (CPC), specifically:

- The Application Bus Interface (ABI) port
- The Agent port
- The Basic Input/Output Services (BIOS) port
- The Task Management Unit (TMU) port
- The Miscellaneous port
- The Standard Agent Interface (SAI) timing diagrams

This document assumes you are familiar with Tarari's Content Processor Development Kit (CP-DK), including the Content Processing Platform (CPP) Board, the software stack, and the CPC.

For more information regarding the above, we recommend that you first read these documents:

- *Content Processor Development Kit Agent Driver Developer Guide*, Tarari part number A02209-001 or later.
- *Content Processing Platform Installation Guide*, Tarari part number A02202-001 or later.

Terms

Table 1 describes terms used in this document.

Term	Description
ABI	Agent Bus Interface
Agent	Acceleration Agent (Anti-Virus, XML, and the like)
CPC	Content Processing Controller: The logic component on the CPP board that acts as a bridge or arbiter between the PCI bus, Agents, and DDR SDRAM
CP-DK	Content Processor Development Kit: a combination of hardware and software content processing building blocks that creates a flexible platform designed to accelerate a variety of compute-intensive algorithms
CPE	Content Processing Engine: either of two reconfigurable logic components on the CPP board
CPP	Tarari's Content Processing Platform, and the board on which it is installed.
DDR SDRAM	Double Data Rate Synchronous Dynamic Random Access Memory: The CPP board's main memory
Dword	A dword (double word) pointer points to 4 bytes of data at a time. For example: Pointer X initially points to bytes 0-3. If it increments by 1, Pointer X points to bytes 4-7.
EOF	End of File
FIFO	First in, first out
LOF	Length of File
Qword	A qword (quad word) pointer points to 8 bytes of data at a time. For example: Pointer Y initially points to bytes 0-7. If it increments by 1, Pointer Y points to bytes 8-15.
SAI	Standard Agent Interface
SOF	Start of File
TMU	Task Management Unit

Table 1: Terms Used in this Document

External Interfaces

The CPC has these main interconnection ports, as Figure 1 shows:

The **ABI port** provides in-band and out-of-band communication channels with the CPC.

The **Agent port** provides a FIFO-type interface with an Agent for in-band data movement.

The **BIOS port** provides a memory mapped I/O interface to the BIOS Controller for reading, writing, and initializing internal memory/registers.

The **TMU port** provides an out-of-band communication channel with the TMU.

The **Miscellaneous port** provides connections for clock, reset, and static configuration data. All SAI interface signals are internal; they connect to other modules, not to package pins.

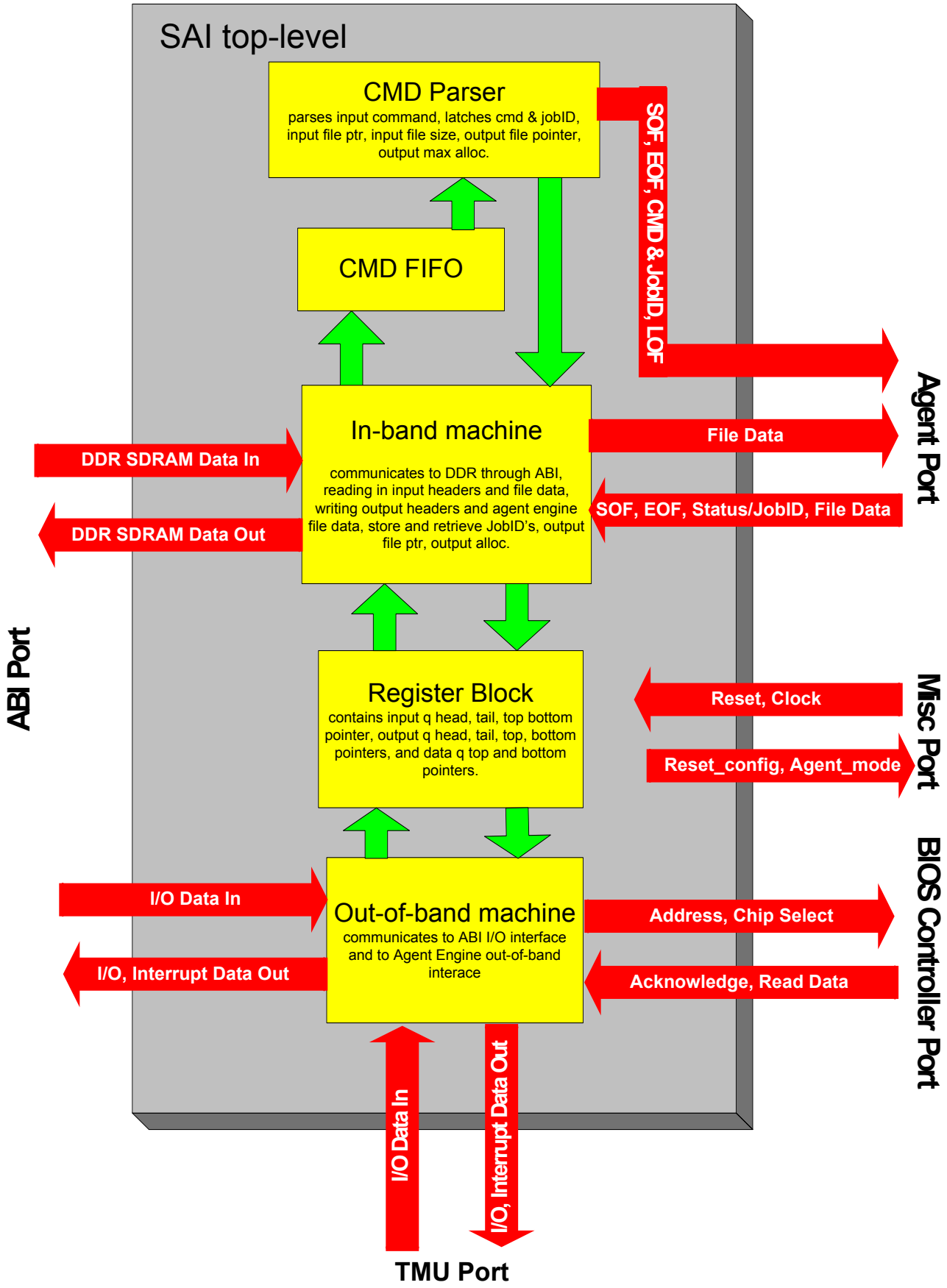

Figure 1: SAI Block Diagram

ABI Port

The SAI communicates with the CPC using the Agent Bus Interface (ABI). This interface allows the SAI to request blocks of data from DDR SDRAM and to write data blocks back to the DDR SDRAM. This interface also provides an out-of-band communications channel with the CPC for hardware initialization/status and for software interrupts. Table 2 lists the signal names and descriptions.

Name	I/O	Width	Description
SABI_REQUEST	O	1	Request transfer to/from ABI
SABI_READ_WRITE	O	1	Read/Write line to determine request type
SABI_ADDRESS	O	25	Starting address of transfer
SABI_LENGTH	O	25	Number of qwords to be transferred
SABI_DTM_AVAIL	O	1	Data available, valid data on SABI_DATA_TO_MEM
SABI_DATA_TO_MEM	O	64	Write data to ABI
SABI_DATA_MASK	O	8	Data mask for write data bus
SABI_IO_DATA_FROM_AGENT	O	32	I/O data to ABI
SABI_IODFA_WRITE	O	1	I/O write data strobe to ABI
SABI_INT	O	1	I/O interrupt strobe to ABI
SABI_DFM_ACCEPT	O	1	Data accept, accept DDR data from ABI
SABI_MEM_XFR_TERM	O	1	Memory transfer terminate
ABIS_DTM_ACCEPT	I	1	Data accept, ABI is accepting data to DDR
ABIS_DFM_AVAIL	I	1	Data available, valid data on ABIS_DATA_FROM_MEM
ABIS_DATA_FROM_MEM	I	64	Read data from ABI
ABIS_IODTA_WRITE	I	1	I/O write data strobe from ABI
ABIS_IO_DATA_TO_AGENT	I	32	I/O data from ABI

Table 2: Agent Bus Interface Port Signals

Agent Port

The Agent Port contains an input FIFO interface and a corresponding output FIFO interface. These steps list the operations of the agent port:

1. The Input FIFO interface pushes data from the DDR SDRAM into the Agent supplied FIFO. The Agent's input FIFO must therefore contain enough storage to receive BS_RD_REQ_SZ words of data, part of the BIOS Controller Port (see "BIOS Controller Port" on page 7).
2. When data is available to transfer to the Agent, and the Agent has asserted AES_RM_AVAIL, the SAI requests BS_RD_REQ_SZ words or less of data from the ABI. The SAI begins the transfer by asserting SAE_SOF with SAE_DVAL, which signifies the command and Job ID (or destination address for common commands) are valid on SAE_DATA. The Agent needs to store the Job ID for use later when it outputs data for this command. The SAI pushes data into the Agent's input FIFO as it receives the data from the ABI.

3. The SAI asserts SAE_DVAL when data is available on the SAI to Agent Port. The last dword of data pushed into the FIFO is indicated by the assertion of SAE_SOF, SAE_EOF, and SAE_DVAL. The Agent must use SAE_BVAL to determine how many bytes are valid in the last dword.
4. Immediately following the SAE_SOF and SAE_EOF phase, SAE_EOF and SAE_DVAL assert, indicating the input file length, in bytes, is on SAE_DATA and the end of that command. The one exception to the protocol is the common command read multiple. Because no file data is supplied to the Agent, there is a SAE_SOF and SAE_DVAL phase in which the command and destination address are on SAE_DATA. The next phase is SAE_EOF and SAE_DVAL, in which the number of words to read for this command is on SAE_DATA.
5. AES_RM_AVAIL is not sampled for a minimum of 2 clocks after the completion of an Input FIFO write. If the input FIFO is almost empty, the Agent asserts AES_ALMOST_MT to request higher priority. The definition of "almost empty" is Agent specific and can be a fixed or software configured threshold as needed.
6. The Output FIFO interface retrieves data from the Agent's supplied output FIFO. The Agent asserts AES_SOF when there is a valid Job ID on AES_DATA.
7. The SAI initiates a write request with the ABI for AES_WORD_CNT words or less of data when AES_WORD_CNT is greater than zero, and there are no outstanding ABI operations. AES_WORD_CNT must not include any SOFs or EOFs, but reflect only the amount of output file data. The word count supplied to the SAI must be masked to a qword count when there are no EOFs in the output FIFO. This constraint is placed on the count because the SAI can only initiate writes to an 8-byte aligned address and write qwords at a time. If the count is not masked to a qword and it is not the final transfer for the command, a 4-byte gap in the output data results in DDR SDRAM. The count can be unmasked once an EOF is pushed into the FIFO, because there are two cases the SAI can encounter:
   - The SAI pulls BS_MAX_WR_SZ number of words from the FIFO if the word count is greater than it. BS_MAX_WR_SZ is a dword count, but is qword aligned so the transfer ends on an 8-byte boundary. If the word count is less than BS_MAX_WR_SZ, this marks the last transfer for the command, and can end on a non-8 byte boundary, because the Agent supplies an output file length in bytes to the host.
   - The SAI asserts SAE_DACCEPT to indicate that it has pulled a word from the FIFO. If the FIFO is not empty, the Agent must then output the next word from its output FIFO. If the output FIFO is nearly full, the Agent asserts AES_ALMOST_FULL to request higher priority. The term "almost full" is Agent specific and can be a fixed or software configured threshold as needed.
8. After the Agent has pushed all of its file data into the output FIFO for the command, the it must then assert AES_SOF and AES_EOF, indicating that the data on AES_DATA is the status and Job ID. The SAI uses this status in the output header which gets written to DDR SDRAM. The Agent must keep these signals asserted until the SAI asserts SAI_DACCEPT.

9. The next phase is AES_EOF, asserted by itself, signifying the end of the transfer and that the output file length in bytes is on AES_DATA. The SAI places this count in the output header.

Table 3 lists the signal names and descriptions.

Direction	Signal Name	I/O	Width	Description
DDR SDRAM to Agent	SAE_SOF	O	1	Start of file. When asserted, the command and Job ID are valid on SAE_DATA, and on last dword on writes, valid for 1 clock.
	SAE_EOF	O	1	End of file, asserted on last data word on writes, and always when IFL is on SAE_DATA.
	SAE_DVAL	0	1	Data Valid, data is valid on SAE_DATA.
	SAE_DATA	0	32	Data bus from SAI to Agent Engine, could contain the command and Job ID, file data, immediate data, or length of the file.
	SAE_BVAL	0	2	Bytes valid. Signifies how many bytes are valid on SAE_DATA. 00 = 4 bytes, 01 = 1 byte, 10 = 2 bytes, 11 = 3 bytes.
	AES_RM_AVAIL	I	1	FIFO room available. Asserts when BS_RD_REQ_SZ + 2 words of space are available in the FIFO.
	AES_ALMOST_MT	I	1	Almost Empty flag. Requests higher priority for the Input FIFO.
Agent to DDR SDRAM	AES_SOF	I	1	Start of file. When asserted, the status and Job ID are valid on AES_DATA
	AES_EOF	I	1	End of file. Asserts with AES_SOF when final status and Job ID are given, and when LOF is valid on AES_DATA.
	AES_ALMOST_FULL	I	1	Flush FIFO, start pulling AES_WORD_CNT of data from FIFO.
	AES_WORD_CNT	I	G	Number of dwords contained in the output FIFO. This count does not include SOF or EOF entries. The G width means VHDL Generic, and is defined by the Agent designer when instantiating the SAI.
	AES_DATA	I	32	Data bus from Agent Engine to SAI. This can contain the Job ID, file data, status, or length of the file.
	SAE_DACCEPT	O	1	Data accept, pull data from output FIFO.

Table 3: SAI to Agent Port Signals

BIOS Controller Port

The BIOS Controller Port reads memory mapped internal registers using the `Agent_Read_Register` out of band command. When this command is decoded by the SAI, it drives the memory address on SB_ADDR and asserts SB_CS. When BS_DATA is valid, the BIOS Controller asserts BS_ACK. The SAI subsequently performs an I/O write to the ABI to complete the operation.

This port also contains RESET, which is a combination of the system and software resets, that must be used to place all registers into a known initial state. Finally, there are 23 bits of dynamic configuration available to the Agent. This dynamic configuration data can be changed by software by issuing an Agent_Config out-of-band command. The Agent defines the use of configuration data. Table 4 lists the signal names and descriptions.

Direction	Name	I/O	Width	Description
SAI to BIOS	SB_ADDR	O	24	Address of out-of-band Peek.
	SB_CS	O	1	Chip select. Signifies that SB_ADDR is valid for out-of-band reads, and is valid for 1 clock.
	RESET	O	1	Global Reset. Must be connected to the direct preset/clear of all Agent's flip/flops. The trailing edge of RESET is synchronous to the rising edge of CLK133. This signal is a combination of the external reset and all software resets.
	SB_DYNAMIC_CFG	O	24	Dynamic configuration for Agent from out-of-band Agent op code Agent_Config.
	SB_SAI_REV	O	4	SAI revision. These must be bits 31:28 of the Agent's revision register.
BIOS to SAI	BS_ACK	I	1	Acknowledge. Signifies that BS_DATA is valid for out-of-band reads, and valid for 1 clock.
	BS_RD_REQ_SZ	I	G	Read request size. The SAI requests this number of 4-byte words when AES_RM_AVAIL is asserted. These must be qword aligned.
	BS_MAX_WR_SZ	I	G	Maximum output FIFO flush size (in dwords) to DDR SDRAM. These must be qword aligned.
	BS_DATA	I	32	BIOS controller data bus. Returns data from out-of-band Peek command, and is valid when BS_ACK is asserted.

Table 4: BIOS Controller Port Signals

TMU Port

The Task Management Unit (TMU) port is similar to the out of band port to the ABI. It allows out of band communications with the TMU, rather than the ABI. Table 5 lists the signals and descriptions.

Name	I/O	Width	Description
TMU_DATA_FROM_AGENT	O	32	I/O data from Agent for I/O writes and interrupts
TMU_IO_WRITE	O	1	I/O write data strobe to TMU
TMU_INT	O	1	I/O interrupt strobe to ABI
TMU_IODTA_WRITE	I	1	I/O write data strobe from TMU
TMU_IO_DATA_TO_AGENT	I	32	I/O data from TMU

Table 5: TMU Port Signals

Generic Port

Table 6 lists the generic port signals.

Name	I/O	Width	Description
CLK133	I	1	133 MHz clock used for all internal and I/O clocking
SYS_RESET	I	1	System Reset. This signal is synchronized with CLK133, and combined with the software resets to produce RESET.

Table 6: Generic Port Signals

SAI Timing

Figure 2 through Figure 7 show the Standard Agent Interface (SAI) timing diagrams. All signals are synchronous to CLK133. Propagation delays, setup, and hold times are determined during FPGA integration and place/route.

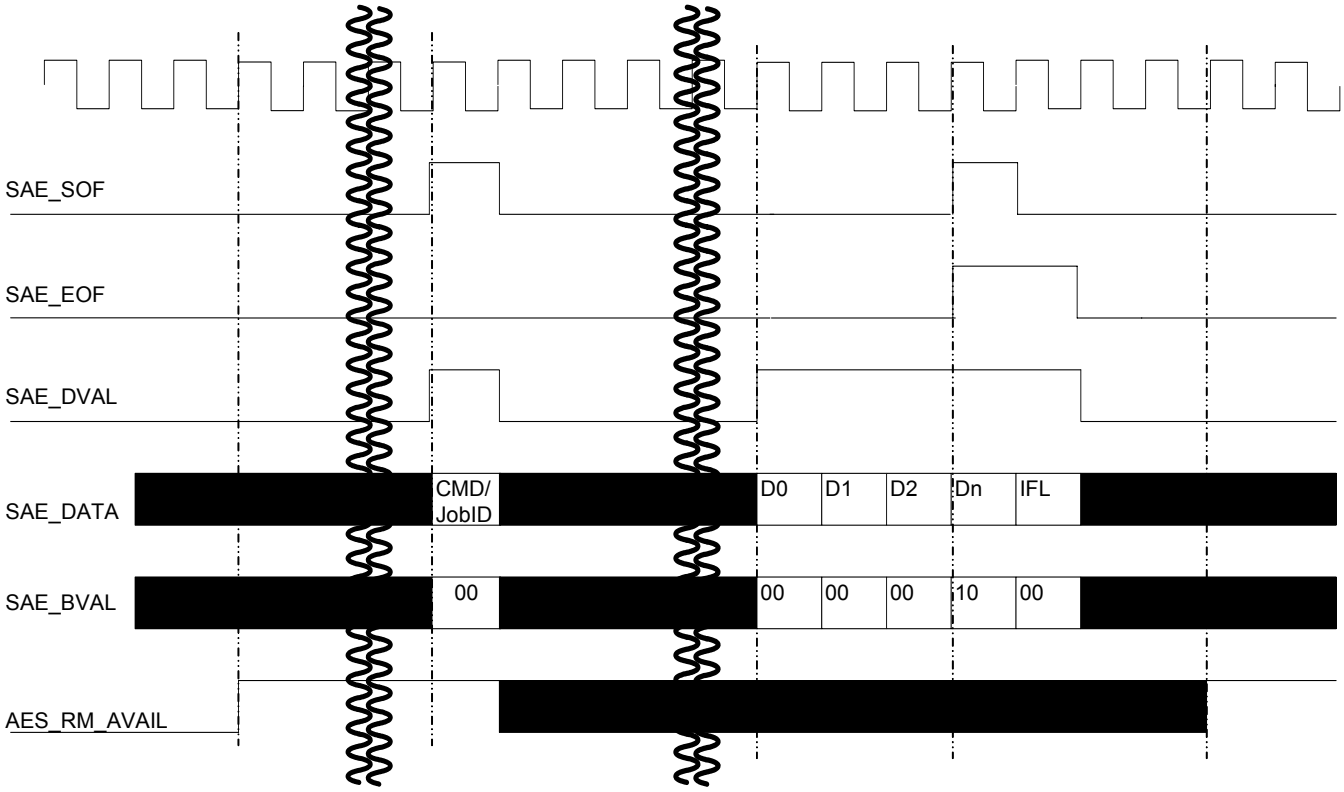

Figure 2: Complete Transfer from SAI to Agent Engine

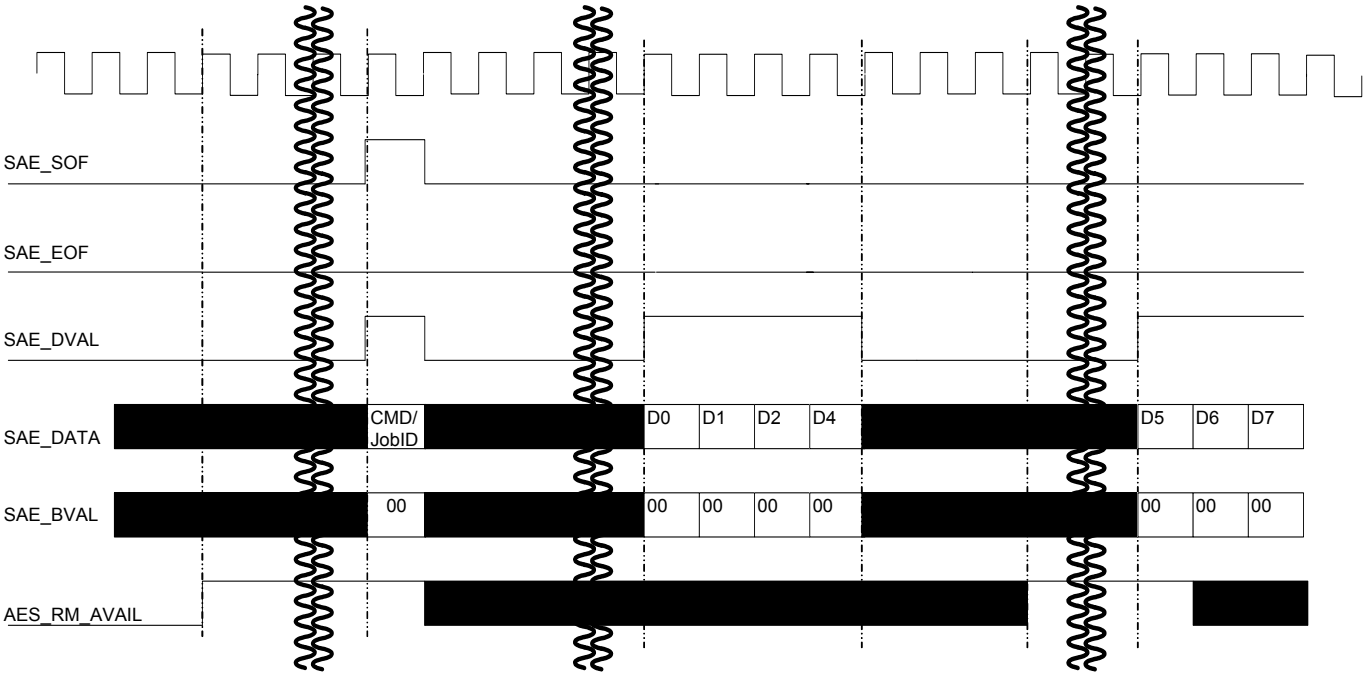

Figure 3: Transfer from SAI to Agent Engine. More Data Needed for Transfer, AES_RM_AVAIL Stays Asserted.

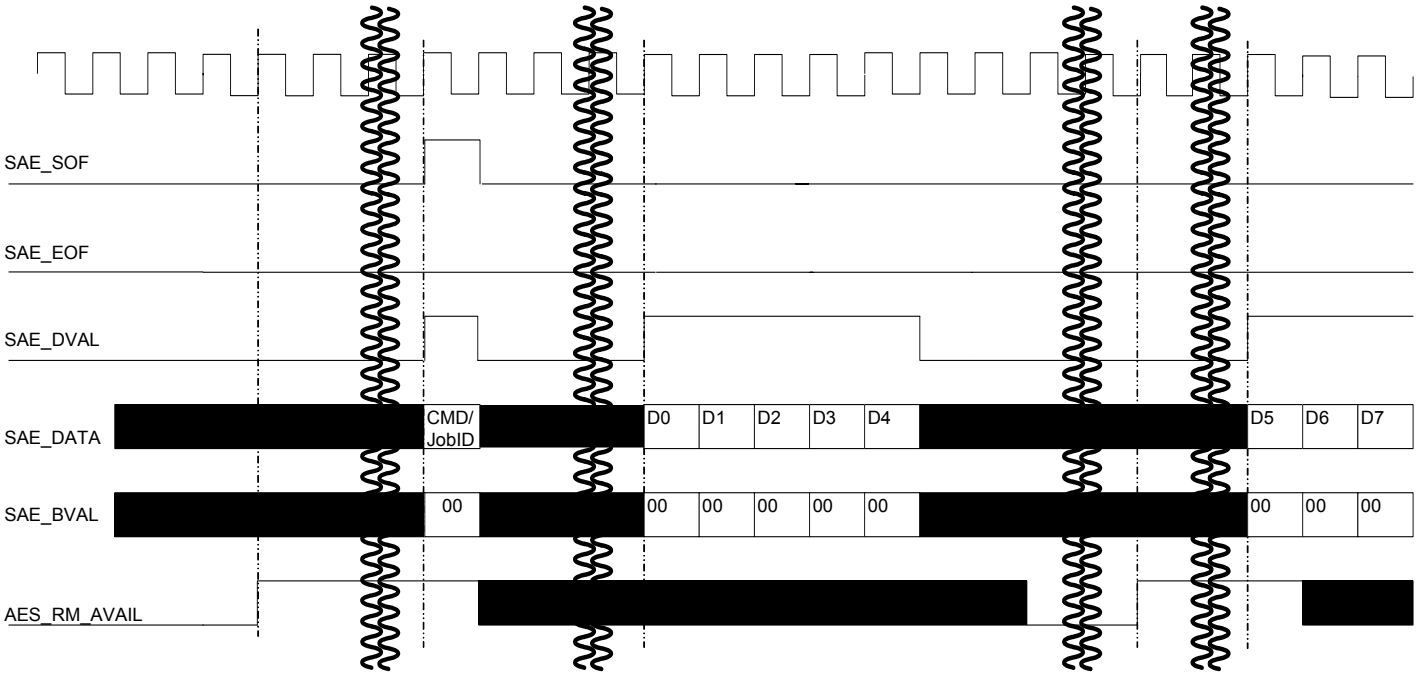

Figure 4: Transfer from SAI to Agent Engine, More Data Needed for Transfer, AES_RM_AVAIL De-asserts.

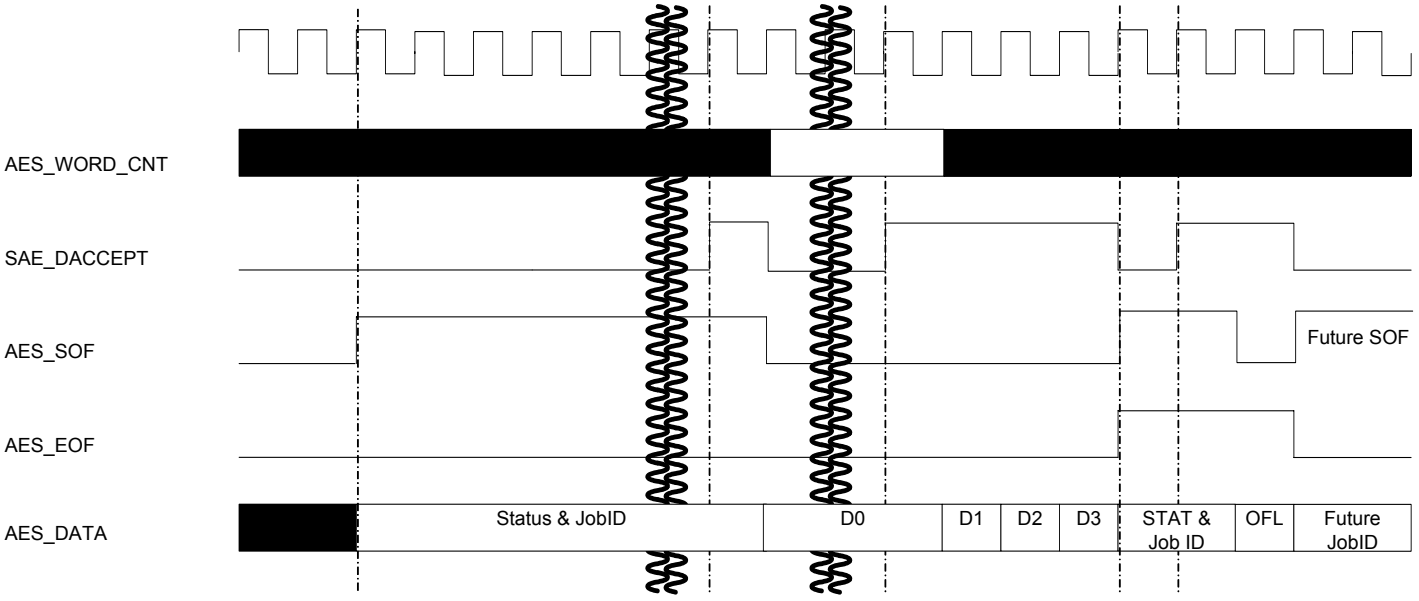

Figure 5: Complete Transfer from Agent Engine to SAI

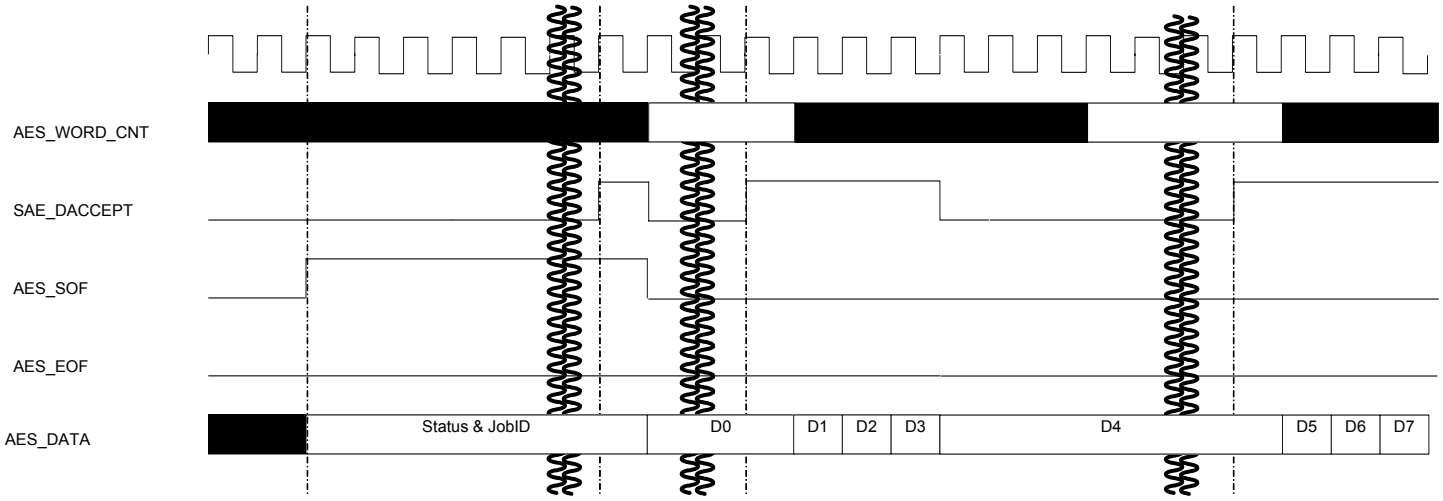

Figure 6: Transfer from Agent Engine to SAI. More Data Required, Wait for AES_WORD_CNT to go Non-zero.

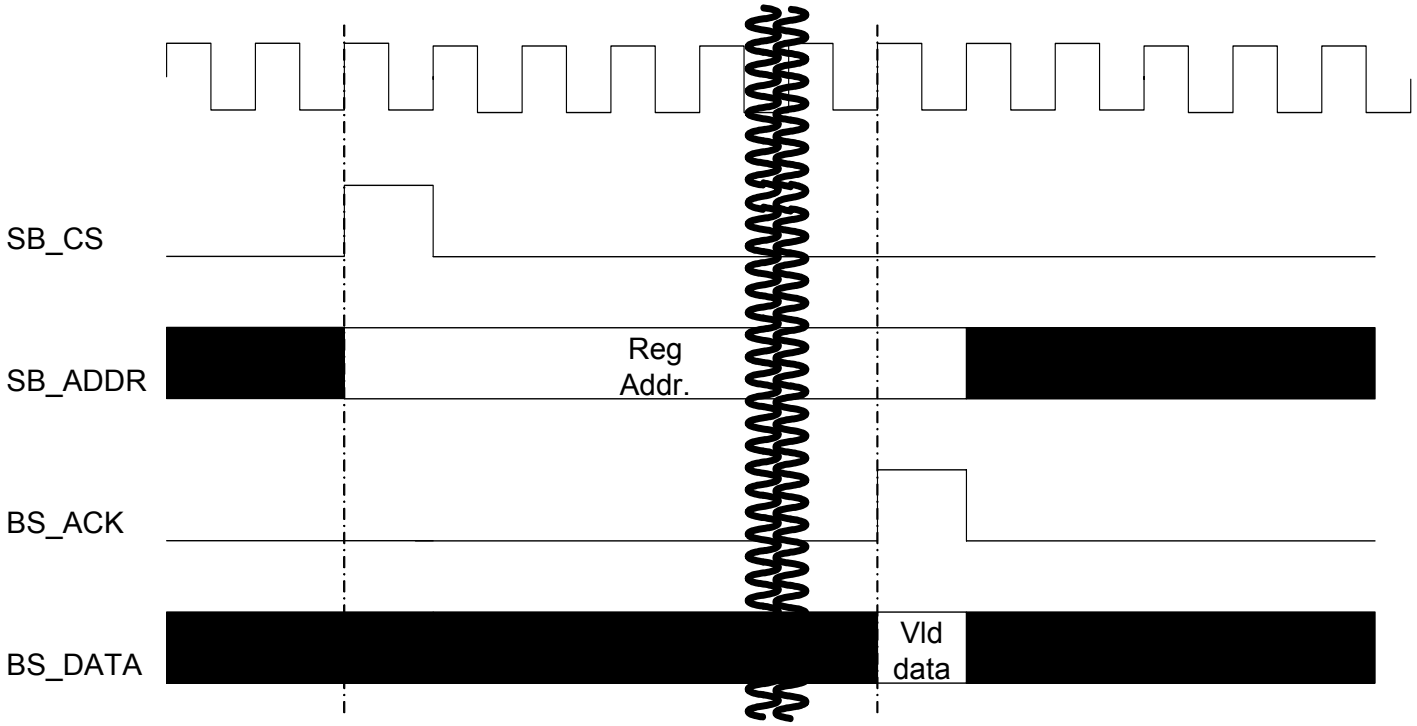

Figure 7: Out-of-band Read from BIOS Controller

Notes